REMARKS

Claim Rejections - 35 U.S.C. § 103

The Examiner has rejected claims 30-31, 33, 36 and 37 under 35 USC 103(a) as being unpatentable over Chau et al. (U.S. Patent No. 5,710,450) in view of Fulford et al. (U.S. Patent No. 5,793,089). The Examiner has rejected claims 34 and 35 under 35 USC 103(a) as being unpatentable over Chau et al. ('450) in view of Fulford et al. "089) as applied to claims 30, 31, and 33 above, and further in view of Subbanna (U.S. Patent No. 5,338,698). The Applicant respectfully traverses. The cited references do not teach or render obvious all of the claimed elements, either individually or in combination. Also, claims 36 and 37 have been cancelled. In particular, the cited references do not teach the claimed elements of independent claim 30 of "a pair of sidewall spacers on opposite sides of the gate electrode, the sidewall spacers having a height of at least 200Å above the third thickness of the gate silicide layer and a width of less than 300Å." In contrast, Chau teaches a first sidewall spacer of an unknown width and second sidewall spacers having a width of between 500Å and 2500Å. Additionally, both Fulford and Subbanna fail to teach sidewall spacers having a width of less than 300Å. The Applicant submits that by forming sidewall spacers having a height of at least 200Å above the third thickness of the gate silicide layer, the volume expanding gate silicide layer may not flow over the barrier formed by the sidewall spacers during hot processing steps. Therefore, sidewall spacers having a width great enough to prevent bridging of the gate silicide over the sidewall spacers are not necessary, and the sidewall spacers claimed by the Applicant may have a width of less than 300Å. Sidewall spacers having a width of less than 300Å are valuable in that they enable the further scaling down of semiconductor devices and allow for the formation of ultrashallow tip regions under the sidewall spacers because dopants only have a short distance to diffuse underneath the gate electrode. Low resistance ultra shallow tip regions allow the fabrication of high performance semiconductor devices. None of the cited references teach the combination of ultrashallow

tip regions and sidewall spacers having a height of at least 200Å and a width of less than 300Å, therefore indicating that such a combination of elements and the specific dimensions are not obvious in light of the cited references.

If there are any additional charges, please charge Deposit Account No. 02-2666.

Respectfully submitted,

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